9.6kbps to 4Mbps IrDA Transceiver

FEATURES

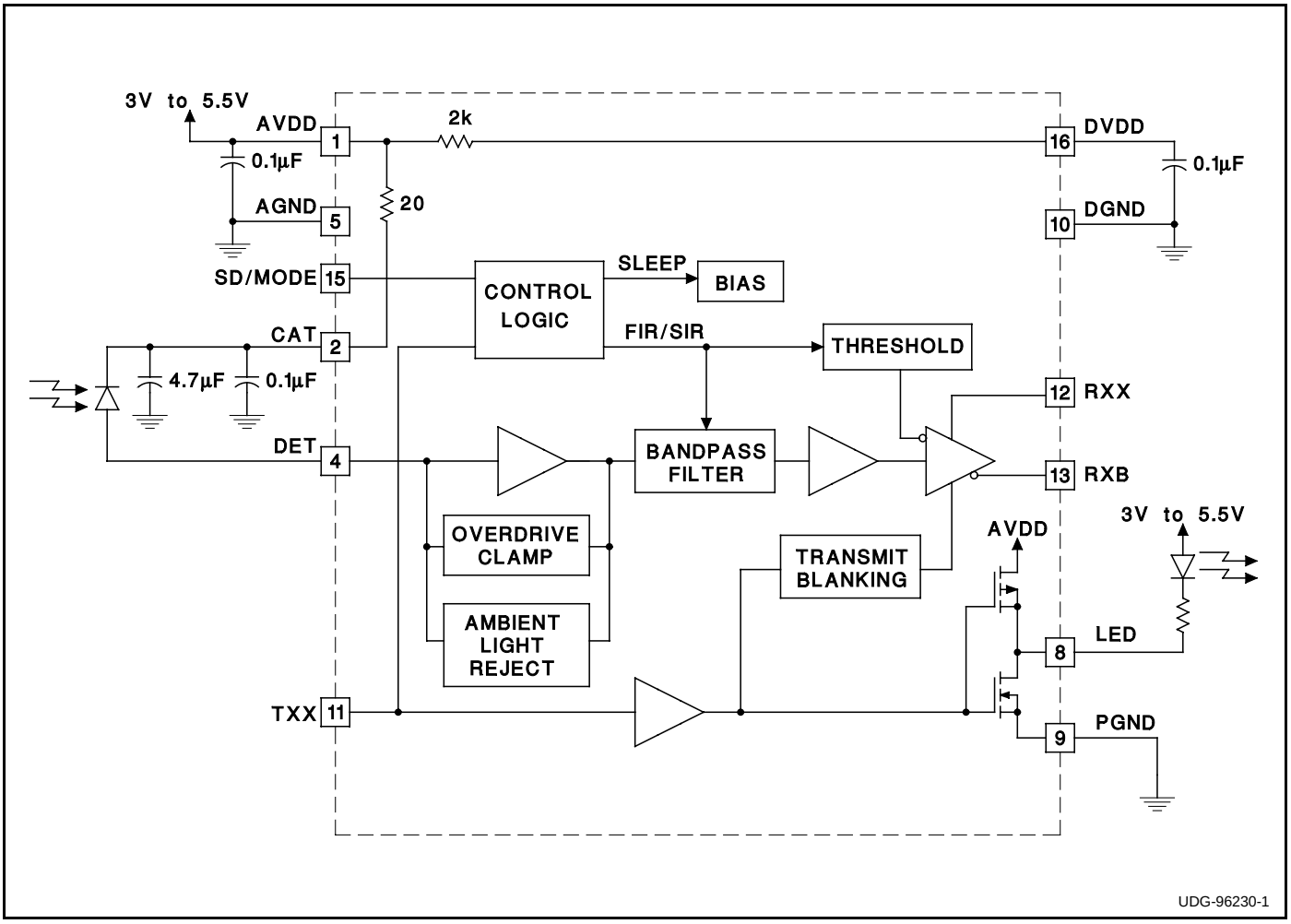
- Supports IrDA 9.6k to 4MBPS Data Rates
- 3.3V and 5V Operation
- Wide Dynamic Receiver Range from 100nA to 100mA
- IrDA Compliant I/O
- 500mA LED Driver
- Low Quiescent Current (Typical 900µA)
- Ultra Low Current Sleep Mode
- Compatible with IrDA Detector Diodes

DESCRIPTION

The UCC5344 IrDA (Infrared Data Association) transceiver supports the analog section of the IrDA standard. The receiver is designed to amplify and condition the signals received by a PIN diode. Bandwidth limiting and ambient light rejection circuitry enhances signal integrity.

The UCC5344 works over a wide supply range of 3.0V to 5.5V and transmission rates from 9.6k to 4MBPS. The transmitter open drain FET is capable of sinking 300mA from 3.3V supplies and 500mA from 5V supplies. The UCC5344 is available in 16-pin DIL and SOIC packages or as tested good die.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

AVDD, DVDD, CAT Voltage . . . . . –0.3V to +7V
SD/MODE, DET, TXX,
LED, DVDD, CAT . . . . . –0.3V to AVDD + 0.3V
I_{RXX}, I_{RXB} . . . . . –10mA to +10mA
I_{DET} 250mA
I_{LED} 1A
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10sec.) . . . . . +300°C

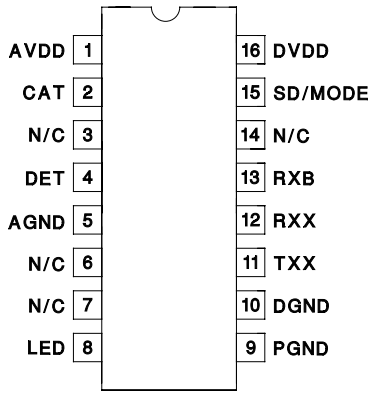
All voltages are with respect to AGND. DGND and PGND must be connected to AGND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

AVDD Voltage . . . . . 3.0V to 5.5V

CONNECTION DIAGRAM

DIL-16, SOIC-16 (Top View)
N Package, D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise specified, T_A = 0°C to 70°C, AVDD = 3.0V to 5.5V, C_{AVDD} = 100nF, C_{DVDD} = 100nF, C_{CAT} = 4.7µF + 100nF, T_A = T_J.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current Section					
I_{AVDD}			0.9	1.5	mA
	SD/Mode = AVDD		0	1	µA
R_{DVDD}	AVDD to DVDD	1.5	2	2.5	kΩ
R_{CAT}	AVDD to CAT	15	20	25	kΩ
Receiver Section, 4 Mbps Mode (Programmed via SD/MODE)					
Input Referred Noise			10		pA/√Hz
Detection Threshold			100	400	nA
Signal to Noise	I_{DET} = 240nA, (I_{AMB} Diode ≤ 30µA)		11.8		A/A
Lower Band Limit	(Note 1)		100		kHz
Upper Band Limit	(Note 1)		8		MHz
Output Pulse Width	I_{DET} = 350nA$_{PK}$ to 100mApk and 0 to 200µADC, 125ns input pulse	110	125	140	ns
DVDD – RXX (V_{OH})	I_{RXX} = –100µA		220	330	mV
RXX (V_{OL})	I_{RXX} = 800µA		200	400	mV
Receiver Section, 115 kbps Mode (Programmed via SD/MODE)					
Input Referred Noise			10		pA/√Hz
Detection Threshold			100	200	nA
Signal to Noise	I_{DET} = 100nA (I_{AMB} Diode ≤ 30µA)		11.8		A/A
Lower Band Limit	(Note 1)		50		kHz
Upper Band Limit	(Note 1)		1		MHz
Output Pulse Width	I_{DET} = 100nA$_{PK}$ to 100mA$_{PK}$ and 0 to µADC, 1.6µs input pulse	1.4	1.6	1.8	µs
Transmitter Section					
I_{TXX}	TXX = 0 to AVDD	–10		10	µA
TXX (V_{IH})	AVDD = 3.3V		1.65	2.2	V
TXX (V_{IL})	AVDD = 3.3V	1.1	1.65		V
TXX (V_{IH})	AVDD = 5.0V		2.5	3.5	V
TXX (V_{IL})	AVDD = 5.0V	1.5	2.5		V
LED	TXX = AVDD = 4.5V, I_{LED} = 500mA		0.3	0.6	V
	TXX = AVDD = 3.0V, I_{LED} = 300mA		0.3	0.6	V
I_{LED}	TXX = 0, LED = AVDD = 5.5V			10	µA

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

AGND: Ground reference for sensitive analog circuits. Connect to ground plane.

AVDD: 3.0V to 5.5V supply pin for sensitive analog circuits. Bypass to AGND with 100nF or 1µF ceramic capacitor.

CAT: Filtered supply for PIN diode cathode. Connected internally to AVDD with a 20Ω resistor. Bypass to AGND with a 4.7µF plus a 100nF ceramic capacitor.

DET: Input to receiver amplifier. Connect to PIN diode anode. Shield with AGND from all other signals, especially RXX and RXB.

DGND: Digital Ground Reference. Connect to ground plane.

DVDD: Supply pin for digital circuits. Internally connected to AVDD with a 2kΩ resistor. Bypass to DGND with a 100nF or 1µF ceramic capacitor.

LED: Open drain of transmit output transistor, connect to LED via current limiting resistor.

PGND: Source of the transmit output transistor. Connect to the ground plane.

RXX and RXB: Output and inverted output of the detect amplifier and buffer, connect to UART. Take care to have matched printed circuit board geometries with respect to DET for distance less than 3 centimeters of the DET.

SD/MODE: Shut down and mode select pin. A logic high on SD/MODE puts the chip into sleep mode. A 100ns pulse on SD/MODE will program the chip for FIR (0.576MBPS to 4MBPS) or SIR (9.6kBPS to 115.2kBPS) mode. TXX = 0 on the falling edge of SD/MODE programs SIR mode. TXX = 1 on the falling edge of SD/MODE programs FIR mode. The chip powers up and wakes up in SIR mode.

TXX: Input to the transmit buffer. Connect to UART.

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